ABSTRACT

The preferred embodiments of the present invention are directed to the selective phase lag and time delay of clock signals within a computer system to compensate for additional parasitic capacitance that may be added to that system because of its open architecture. More particularly, the preferred embodiments are directed to clock signal path circuits where each circuit has multiple signal paths of varying lengths. By allowing the clock signals to propagate along a particular path, phase lag or time delay is added to those clock signals. Selection of a particular path for the clock signal is made by activating electrically controlled switches which themselves are activated or deactivated by software programs that run during power-up of the computer system that determine required phase lag or time delay of those clock signals as a function of parasitic capacitance in the computer system.